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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRAN, MAI HUONG C	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 08/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,798	TU ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11,12 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11,12 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

This Office Action is in response to Amendment filed on 07/27/2005.

Claims 1-9, 11, 12 and 28 are presented for examination.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 7, 9, 11, 12, and 28 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,368,976 to Yamada.

Regarding to claim 1, Yamada discloses a split gate flash memory cell structure comprising a semiconductor region 1 within a substrate extending to a surface; a gate insulator layer 2 formed over the semiconductor surface 1; a conductive floating gate 9 disposed over the gate insulator layer 2; a floating gate insulator layer 8 disposed over the floating gate 9; sidewall insulator spacers 21 disposed along bottom portions of sidewalls of the floating gate 9 on the gate insulator layer 2; an intergate insulator layer 23 disposed over exposed portions of the gate insulator layer 2, the floating gate insulator layer 8 and

the sidewall insulator spacers 21; and a conductive control gate 26 disposed over the intergate insulator layer 23 and covering a portion of the floating gate 9 (col. 4, lines 35-67, cols. 5, 6 and figs. 1-5).

Regarding to claim 2, the structure wherein the semiconductor region is a silicon region (col. 1, lines 19-20).

Regarding to claim 3, the structure wherein the substrate is a silicon containing substrate (col. 4, lines 19-20).

Regarding to claim 7, the structure wherein the spacer insulator layer is an oxide layer (col. 5, lines 29-45).

Regarding to claim 9, the structure wherein the spacer insulator layer is a deposited oxide layer (col. 5, lines 57-64), the gate insulator layer is a thermal oxide layer (col. 1, lines 19-21), and the floating gate insulator layer is a polysilicon oxide layer (col. 1, lines 39-48).

Regarding to claim 11, the structure wherein the intergate insulator layer is an oxide layer (col. 5, lines 65-67, fig. 4).

Regarding to claim 12, the structure wherein the conductive control gate is composed of polysilicon (col. 6, lines 9-10, and fig. 5).

Regarding to claim 28, Yamada discloses a split gate flash memory cell structure comprising a semiconductor region 1 within a substrate extending to a surface; a gate insulator layer 2 formed over the semiconductor surface 1; a conductive floating gate 9 disposed over the gate insulator layer 2, the gate insulator layer 2 extending outside of the conductive floating gate 9 (fig. 5); a floating gate insulator layer 8 disposed over the floating gate 9; sidewall insulator spacers 21 disposed along bottom portions of sidewalls of the floating gate 9 adjacent the gate insulator layer 2; an intergate insulator layer 23 disposed over exposed portions of the gate insulator layer 2, the floating gate insulator layer 8 and the sidewall insulator spacers 21; and a conductive control gate 26 disposed over the intergate insulator layer 23 and covering a portion of the floating gate 9 (col. 4, lines 35-67, cols. 5, 6 and figs. 1-5).

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention

was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-5 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,368,976 to Yamada in view of Lin (6,620,689).

Regarding to claim 4, Yamada discloses the claimed invention except for the structure wherein the gate insulator layer is a thermally grown oxide layer grown to a thickness of about 50 to 200 angstroms. However, Lin discloses the structure wherein the gate insulator layer is a thermally grown oxide layer grown to a thickness of about 50 to 200 angstroms (col. 3, lines 50-52 and col. 4, lines 32-34, figs. 2A-2D).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the structure wherein the gate insulator layer is a thermally grown oxide layer grown to a thickness of about 50 to 200 angstroms, as taught by Lin in order to provide a method of fabricating a flash memory cell characterized by improvement of tip discharge efficiency (col. 2, lines 62-64).

Regarding to claim 5, Yamada discloses the claimed invention except for the structure wherein the conductive floating gate is composed of polysilicon. However, Lin discloses the structure wherein the conductive floating gate is composed of polysilicon (col. 1, lines 53-55, col. 2, lines 8-9, and figs. 1A-1D).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the structure wherein the conductive floating gate is composed of polysilicon, as taught by Lin in order to provide a method of fabricating a flash memory cell characterized by improvement of tip discharge efficiency (col. 2, lines 62-64).

Claim 6 is rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,368,976 to Yamada in view of Guterman et al. (6,002,152).

Regarding to this claim, Yamada discloses the claimed invention except for the structure wherein the floating gate insulator layer is a grown polysilicon oxide layer grown to a thickness of about 800 to 2000 Angstroms. However, Guterman discloses the structure wherein the floating gate insulator layer is a grown polysilicon oxide layer grown to a thickness of about 800 to 2000 Angstroms (col. 25, lines 42-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the structure wherein the floating gate insulator layer is a grown polysilicon oxide layer grown to a thickness of about 800 to 2000 Angstroms, as taught by Guterman in order to produce high capacity FLASH memory devices which use split-gate, source-side hot electron programming, in place of the more conventional drain-side channel hot electron mechanism (col. 2, lines 27-32).

Claim 8 is rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,368,976 to Yamada in view of Chuang et al. (6,855,966).

Regarding to this claim, Yamada discloses the claimed invention except for the structure wherein the spacer insulator layer is a PECVD oxide layer. However, Chuang discloses the structure wherein the spacer insulator layer is a PECVD oxide layer (col. 3, lines 41-51).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the structure wherein the spacer insulator layer is a PECVD oxide layer, as taught by Chuang in order to have a non-volatile memory device with the speed of memory erasure is fast and with a low electric consumptions (col. 1, lines 22-37).

Response to Arguments

Applicant's arguments with respect to claims 1-9, 11, 12 and 28 have been considered but are moot in view of the new ground(s) of rejection.

Applicants argue that because Hsieh discloses the gate oxide layer (120) is removed in the process of etching of the polysilicon (130), the gate oxide layer (120) is only exist under the floating gate (130). Thus, the nitride spacers (195) are formed on the substrate (100) not on the gate oxide layer (see Figs. 2h-2j).

The Examiner agrees with the applicants that Hsieh does not teach the amended claim 1 with sidewall insulator spacers disposed along bottom portions of sidewalls of said floating gate on said gate insulator layer.

However, Yamada has overcome those arguments with the new ground(s) of rejection. For the above reasons, it is believed that the rejections should be sustained. Feature of an invention not found in the claims can be given no patentable weight in distinguishing the claimed invention over the prior art.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Friday from 8:00 AM to 4:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

MK

Mai-Huong Tran